PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 10030775-1

Application Number	Filed
10/736,438	12/15/2003

First Named Inventor: Hildebrant

Art Unit	Examiner
2112	Rizk, Samir Wadie

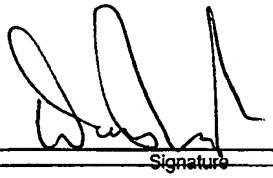
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 47,034
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____



Signature

David Rodack

Typed or printed name

(770) 933-9500

Telephone number

November 07, 2007

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Hildebrant

Serial No.: 10/736,438

Filed: 12/15/2003

Confirmation No.: 3423

Group Art Unit: 2112

Examiner: RIZK, Samir Wadie

Docket No. 10030775-1

For: **Systems and Methods for Adaptively Compressing Test Data**

REMARKS IN SUPPORT OF PRE-APPEAL BRIEF CONFERENCE

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant submits the following remarks in support of a Request for a Pre-Appeal Brief Conference.

REMARKS

Claims 12, 13, 15, 16, 28, 29, 31, and 32 have been rejected in the final Office Action (presumably under 35 U.S.C. 103(a), see reference to petition below) dated August 7, 2007. An Advisory Action was mailed on October 19, 2007 responding to Applicant's response after final and maintaining the rejection. For purposes of the pre-appeal brief conference, Applicant respectfully traverses this rejection as applied to claims 12, 13, 15, 16, 28, 29, 31, and 32, and respectfully submits that there exists clear cases of error, supported by the evidence in the record, in this rejection.

Also, Applicant has filed simultaneously with the pre-appeal brief conference a petition to the Director under 37 C.F.R. 1.181 to request withdrawal of the final rejection based, at least in part, on the ambiguity in the grounds for rejection.

I. Rejection of Independent Claim 12

The final Office Action alleges the following on page 3 (no emphasis added):

> The Examiner re-iterates that Wang in FIG. 1, reference characters (110) and (113) teaches combinational logic test pins. Combinational logic is inherently non-clock signals to those of ordinary skill in the art. Also, Wang in FIG 1, reference characters (108), (109) and (111) teaches SC "Scan Chain" test pins. Scan chain is inherently clock signals to those of ordinary skill in the art.

Applicant believes the inherency argument proferred in the final Office Action has been adequately traversed, and hence believes the continued rejection as evidenced by the Advisory Action to be based on clear legal error. Even assuming *arguendo Wang* teaches scan chains, *Wang* does not disclose that the test pins 108, 109 and 111 are ***clock pins***. In response to the conclusory allegation reproduced above in association scan chain logic, Applicant has searched for and subsequently reviewed several web-articles to confirm whether there is support for the above allegations. Exhibits A-B are incorporated herein as

part of the pre-appeal brief conference, two of which were referenced on page 9 in the response to final Office Action filed October 5, 2007 (a third article referenced in the last response is no longer available on the Internet). In particular:

Exhibit A is a technical paper retrieved over the Internet via http://www.ics.uci.edu/~nodari/vts2003.pdf, entitled, "A Reconfigurable Shared Scan-In Architecture;"

Exhibit B is a power point presentation retrieved over the Internet via http://www.caip.rutgers.edu/~bushnell/dsdwebsite/dsdlecture26.ppt, and entitled, "332:437 Lecture 26 IEEE Boundary Scan Standard Test & System Test."

Upon review of these articles, Applicant has found no evidence to support the Examiner's unsupported conclusion that a "scan chain is inherently clock signals." Quite the contrary, the inputs to the scan chains described and shown in the articles referenced above appear to be non-clock signals.

Further, as also set forth on page 9 of the after final response, even assuming *arguendo* evidence can be presented to support clock signal inputs to a scan chain, that evidence alone (in view of other literature such as disclosed above) cannot support an inherency argument since, as set forth in a recent Federal Circuit court decision:

> "[A]nticipation by inherent disclosure is appropriate only when the reference discloses prior art that must necessarily include the unstated limitation." *Atofina v. Great Lakes Chemical Corp.*, 441 F.3d 991, 1000 (Fed. Cir. 2006).

Additionally, Applicant respectfully submits that there is clear factual error in the Advisory Action. In particular, the Advisory Action makes reference to "clocked pins" allegedly shown in the reference when the claim language clearly recites clock-pins and non-clock pins.

Accordingly, Applicant respectfully requests that the rejection to claim 12 be withdrawn.

II. Rejection of Independent Claim 28

The final Office Action fails to adequately address the features of claim 28, and the Advisory Action appears to focus on clock***ed*** pins and what *Wang* allegedly teaches. For purposes of this response, Applicant addresses the rejection based on similar arguments presented for claim 12. In particular, the final Office Action alleges the following on page 3 (no emphasis added):

> The Examiner re-iterates that Wang in FIG. 1, reference characters (110) and (113) teaches combinational logic test pins. Combinational logic is inherently non-clock signals to those of ordinary skill in the art. Also, Wang in FIG 1, reference characters (108), (109) and (111) teaches SC "Scan Chain" test pins. Scan chain is inherently clock signals to those of ordinary skill in the art.

Applicant believes the inherency argument proferred in the final Office Action has been adequately traversed, and hence believes the continued rejection as evidenced by the Advisory Action to be based on clear legal error. Even assuming *arguendo Wang* teaches scan chains, *Wang* does not disclose that the test pins 108, 109 and 111 are ***clock pins***. In response to the conclusory allegation reproduced above in association scan chain logic, Applicant has searched for and subsequently reviewed several web-articles to confirm whether there is support for the above allegations. Exhibits A-B are incorporated herein as part of the pre-appeal brief conference, two of which were referenced on page 9 in the response to final Office Action filed October 5, 2007 (a third article referenced in the last response is no longer available on the Internet). In particular:

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Upon review of these articles, Applicant has found no evidence to support the Examiner's unsupported conclusion that a "scan chain is inherently clock signals." Quite the contrary, the inputs to the scan chains described and shown in the articles referenced above appear to be non-clock signals.

Further, as also set forth on page 9 of the after final response, even assuming *arguendo* evidence can be presented to support clock signal inputs to a scan chain, that evidence alone (in view of other literature such as disclosed above) cannot support an inherency argument since, as set forth in a recent Federal Circuit court decision:

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Additionally, Applicant respectfully submits that there is clear factual error in the Advisory Action. In particular, the Advisory Action makes reference to "clocked pins" allegedly shown in the reference when the claim language clearly recites clock-pins and non-clock pins.

Accordingly, Applicant respectfully requests that the rejection to claim 28 be withdrawn.

In view of the foregoing, Applicant respectfully submits that the art of record does not anticipate or make obvious claims 12 or 28 (and dependent claims 13, 15, 16, 29, 31, and 32), and the rejection to the same is clearly improper due to errors and/or omissions by the Examiner.

CONCLUSION

Favorable reconsideration and allowance, or the re-opening of prosecution on the merits, of the present application and claims 12, 13, 15, 16, 28, 29, 31, and 32 are hereby courteously requested.

Respectfully submitted,

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

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